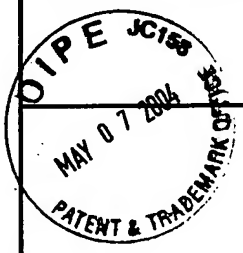
CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8) Applicant(s): Douglas R. Hackler, Sr. et al.			Docket No. 51889/2
Serial No. 10/612,169	Filing Date July 3, 2003	Examiner Phat X. Cao	Group Art Unit 2814

Invention: **MULTI-CONFIGURABLE INDEPENDENTLY MULTI-GATED MOSFET**



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Douglas R. Hackler Sr., et al. Confirmation No. 9150

Application No. 10/612,169

Filed: July 3, 2003

For: **MULTI-CONFIGURABLE INDEPENDENTLY MULTI-GATED MOSFET**

Group Art Unit: 2814

Examiner: Phat X. Cao

Date: May 3, 2004

RESPONSE TO RESTRICTION REQUIREMENT

TO THE COMMISSIONER FOR PATENTS:

Applicant responds as follows to the April 4, 2004, Office Action requiring an election of species.

Claims 1-44 are in the application. Claims 1, 9, 17, 28, 31, 34 are in independent form. The claims stand subject to restriction under 35 USC § 121. The Examiner states that restriction to one of the following species of claims is required:

I. Claims 9-16; and

II. Claims 1-8 and 17-44.

Applicant provisionally elects, with traverse, to prosecute claims 1-8 and 17-44.

Applicant respectfully traverses the Examiner's restriction requirement for the following reasons. The Examiner states that "in the process claim 9, instead of first forming a channel and a bottom gate and then forming a gate insulator on the channel and a top gate on the gate insulator, the top gate and the gate insulator can be formed first and then forming the channel and the bottom gate consecutively on the gate insulator and the top gate." The Examiner appears to

rely on MPEP § 806.05(f) to support the restriction requirement on the grounds "that the product as claimed can be made by another and materially different process."

The Examiner's position that the product can be made by another and materially different process is not feasible due to materials and physics restrictions defined by nature. The present invention is directed to a field effect transistor. This technology is not a macro level fabrication that involves stacking various materials, but is a microelectronics fabrication technology. For example, a basic SOI silicon layer is generally less than 2000 angstroms in total thickness. The channel and bottom gate layers are built in this very thin silicon by manipulating the material properties of the silicon, thereby changing the silicon material properties to create what are loosely referred to in the industry as "layers."

The suggestion that the layers can be interchanged at will to provide an alternative method of fabrication is not feasible. The suggested concept of forming the top gate and the gate insulator first and then forming the channel and the bottom gate consecutively on the gate insulator and top gate cannot meet the material requirements for functional solid state semiconductor devices. The bottom gate and channel are semiconductors. The gate insulator is a dielectric, and the top gate is a metal or metal equivalent. Dielectrics and metals are not semiconductors. Semiconductor substrates cannot be formed on insulators or metals.

The bottom gate forms a semiconductor device that is located adjacent to the substrate and is formed before any top gate processing. In fabrication, the bottom gate is exposed to high temperatures to anneal the silicon lattice and activate the electrical characteristics of the device. The metal material of the top gate cannot tolerate the high temperature anneal required for bottom gate formation.

The gate insulator is an even more extremely thin layer than the top gate. The gate insulator must be of extremely high quality and cannot be exposed to possible contamination to meet the breakdown voltage requirements on which the electrical performance is based. The fabrication of the bottom gate after formation of the top gate would require gate insulator exposure to bottom gate dopants and damage gate insulator integrity.

The bottom gate (on the bottom of the device) and the top gate (on the top of the device) are not random locations. The subsequent novel, unique and proprietary interconnect architecture requires the materials and gates to be in the locations specified in order to meet contact feasibility requirements.

It is not only the Applicant's position, but a physical reality that the product as claimed cannot be made by another and materially different process. The Applicant has not been shown a viable alternative process, and this restriction requirement is improper.

Furthermore, the Manual of Patent Examining Procedure § 803.01 recites that "[i]f the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to distinct or independent inventions." Process claims 9-16 track the fabrication of a product recited in the remaining claims. Process claims 9-16 are not directed to a distinct or independent invention and certainly do not represent a serious burden to examination.

Applicant, therefore, requests the Examiner to withdraw the restriction requirement.

Respectfully submitted,

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